CEN/CLC/JTC 22/WG 3 "Quantum Computing"
WG Secretariat: AFNOR
Convenor: Jean-Baptiste Latre

Narrowing Scope of Layer Model

Document type	**Meeting**	**Document date**	**Expected action**
Contribution	JTC22-WG3-014	2024-05-22	For decision

Title	Narrowing Scope of Layer Model
Author	Oskar van Deventer (TNO) Rob van den Brink (Delft Circuits) Angie Qarry (QDeepTech) Michael Fellner (ParityQC)
Organisation	TNO
Representing	NEN
Work Item number	JTC22004
Work Item title	Layer model of Quantum Computing
Summary	This document proposes a narrowing of the scope of the TR on Layer Model for Quantum Computing. A text proposal is included.
Motivation	The progress on the layer model seem to be a bit stuck at the moment. The latest agreed draft (v0.3) is CEN-CLC-JTC 22-WG 3_N45, was at the Turin meeting on 21 November 2023. The issue was discussed at JTC22WG3-013 on 17 May 2024. Contribution CEN-CLC-JTC 22-WG 3_N74_Rescoping-of-Layer-Model discussed various options for rescoping. The meeting showed consensus that a narrowing of the scope would be the way forward, albeit with many details still needing to be fleshed out. The text proposal at the next page includes some new editor's notes that reflect comments received at the WG3 meeting. The document can only be put forward for ballot after all editor's notes have been addressed and removed. This should provide reassurance that these comments will be addressed some time.
Details	See next page

Proposal (instruction to the editor, using change marks)

CHANGE 1: Change the title of the document as follows

JTC 22 WG3 Quantum Computing
Layer Model of universal gate-based Quantum Computing

CHANGE 2: Change the Scope section as follows

1 Scope

This document describes a layer model that covers the entire stack of ~~a quantum computer~~ universal gate-based quantum computers. The group of lower-level (hardware) layers are organized in different hardware stacks tailored to different hardware architectures, while the group of higher-level (software) layers are built on top of these and expected to be common for all quantum computing systems. The higher-up in the stack, the more agnostic it will be from underlying layers. Reducing the dependencies between higher and lower layers is a crucial point for optimized quantum computations. A co-requisite point is to allow for a free but well-defined flow of information up and down the higher and lower layers to allow for co-designing hardware and software.
The scope of this document is limited to a *universal gate-based* quantum-computing model, also known as a digital or circuit quantum-computing model, on multiple physical systems such as transmon, spin-qubit, ion-trap, neutral-atom, and other. This limitation keeps technologies like the universal adiabatic quantum-computing model, and its heuristic form quantum annealing, as out of scope. Moreover, this limitation keeps quantum computing models that are not universal, such as quantum simulators and special purposes, as out of scope. Limiting the scope to a universal gate-based quantum computing model is justified by expected commonalities at the higher layers, mainly above the hardware abstraction layer (HAL) up to the application layer. These commonalities imply a market for software products usable for this wide range of quantum computing technologies.

This document is limited to a high-level (functional) description of the layers involved. Additional details of the individual layers will be described in other, ~~future,~~ future CEN/TRs.

Editor's note: Whereas quantum-computing technologies that are not "universal gate-based" are out of scope of the present document, proponents of such technologies are welcome to develop dedicated layer models for those in a dedicated Work Item.
Editor's note: It was remarked at the WG3 meeting of 17 May 2024 that the scope of the present document could potentially be narrowed down even further. Any proposal for this can be submitted as contribution to the present WG3 Work Item.
Editor's note: It was remarked at the WG3 meeting of 17 May 2024 that the present document would benefit from documentation of the abstract computing model for universal gate-based quantum computers, complementary to hardware layer descriptions. Contributions on this are welcome.
Editor's note: The document (e.g. section 4, section 5.5) may need to be checked about photonic quantum computing, as not all classes of photonic quantum computing are "universal". Contributions on this are welcome.
Editor's note: The document (e.g. section 9, section 10) may need to be checked about quantum annealing, which is not "universal gate-based". Most likely that section needs to be revised such that only a single computing model is described. Contributions on this are welcome.
Editor's note: It was remarked at the WG3 meeting of 17 May 2024 that more details are needed on software modularity ("upward compatibility"?). Contributions on this are welcome.
Editor's note: It needs to be clarified to what extent "the universal one-way quantum computing model known as cluster state, and the universal variational quantum computing model known as a hybrid" (measurement-based quantum computing or variational quantum computing) are within or outside the scope of the present document. Contributions on this are welcome.

CHANGE 3: Extend the Terminology section as follows

3.1 Terminology

Codesign - A design approach where (software) modules query lower layers for identifying the (hardware) capabilities and limitations of a system and subsequently tailor their behaviour to these capabilities and limitation. This approach allows for hardware-specific optimizations and adaptations to optimize quantum computations.

Gate-based quantum computing - A gate-based quantum computer processes a sequence of instructions (called a quantum circuit) to change the state of a quantum register with many qubits before the resulting state is queried by measurements. The instructions may comprise gates, mid-circuit measurements and state preparations. Gates are unitary operations acting on a set of qubits. A gate-based quantum computer can be characterized by a gate set, wherein the gate set is composed of gates which can be performed by the quantum computer.

Universal gate-based quantum computing - A universal quantum computer is defined as a quantum computer being capable of processing an arbitrary quantum circuit. A universal gate-based quantum computer must have a gate set which is universal. A gate set is said to be universal if any unitary operation may be approximated to arbitrary accuracy by a quantum circuit involving only those gates [Nielsen & Chuang, Quantum Computation and Quantum Information]. The definition also comprises non-fault-tolerant universal quantum computers, which can process an arbitrary quantum circuit reliably only up to a certain length, size or gate count.

Editor's note: Please include the cited reference in the Bibliography section.

CHANGE 4: Change the HAL section as follows

7 Hardware abstraction Layer (HAL)

The aim of the Hardware Abstraction Layer for universal gate-based quantum computers is to inform higher layers with capabilities and limitations supported by the underlying hardware. Layers above the HAL can use this information to hide many implementation-specific details to higher layers by offering a more unified interface. Layers above may also use this information to provide higher-level commands to programmers or programs allowing for implementing hardware-specific optimizations and adaptations. Not all quantum computers make use of the same paradigm. Annealing quantum computers behave differently from gate-based quantum computers, and therefore their HALs might be different as well. The HAL can therefore provide information about the underlying architecture, such as for instance being "gate-based", "annealing" or "simulation".

~~7.1HAL for gate-based quantum computers~~

A gate-based quantum computer processes a sequence of instructions to change the state of a quantum register with many qubits before the resulting state is queried by measurements. A convenient graphic representation of such a sequence has the appearance of a circuit where the elements seem to operate on one or more qubits simultaneously. Due to this convenient graphic representation, these instructions are called gates.

Editor's note: It may be useful to add text on "universal". Contributions are welcome.

7.~~1.~~1 Organization of qubits

<content not changed>

7.~~1.~~2 The concept of native gates

<content not changed>

7.~~1.~~3 Concept of primitive gates

<content not changed>

7.~~1.~~4 Concept of measurement

<content not changed>

7.~~1.~~5 Interfacing considerations

<content not changed>

~~7.2HAL for annealing quantum computers~~

~~EDITORIAL NOTE: Contributions are invited for adequate text that should fit here.~~

~~7.3HAL for simulation of quantum physics models~~

~~EDITORIAL NOTE: Contributions are invited for adequate text that should fit here.~~
