# Chapter 3
# Extraction of transfer parameters

The quantification of parasitics, as discussed in section 1.2.3, is of basic importance for wideband feedback design. Extraction of parameter values from measurements is a robust approach to quantify parasitics.
Low frequency measurements, usually below 1 MHz, are often used to estimate device parasitics. The application of estimated parameters from low frequency measurements are restricted to simplified device models. They may fail, however, for complex devices such as transistors and at 'high' frequencies.
This chapter introduces some new and powerful extraction methods to model devices from measured data, using equivalent circuits that include parasitic interactions. Examples demonstrate the applicability of this work to semiconductor devices such as photo-diodes and transistors. All discussions are focused on *linear* measurements and modeling.

***Highlights of this chapter***
The highlights of this chapter, which have been explored in this study, are:

- Development of a robust algorithm to fit rational functions with measured transfer functions (magnitude and phase). The iterative method is simple and requires no starting values. Further, various related algorithms are developed for extracting rational functions when transfer information is incomplete. For instance, spectral measurements performed with spectrum analyzers and white noise as stimulus are scalar in nature, so that phase information is lacking.
- Development of a robust algorithm to extract simple transistor models (BJT's and FET's) from measured two-port parameters for synthesis purposes. The method is significantly simpler than four-dimensional brute-force methods, as for instance are implemented in circuit simulators such as Touchstone© [124].
- Discrepancies found between measurements and the widely accepted theory [406] that diffusion capacitance is the dominant factor in limiting the transition frequency of bipolar transistors. The two-port measurements we performed and the measurements specified by semiconductor manufacturers indicate that diffusion capacitance might be a quantity of minor importance in wideband BJT's.
- Development of a simple (linear) bipolar junction transistor model, that is adequate for synthesis purposes and valid for frequencies up to the transition frequency $f_T$. This is a significant improvement compared to conventional models based on diffusion capacitance concepts. Conventional models are inadequate for frequencies in excess of 10% of $f_T$.

This chapter provides a theoretical foundation for the rest of this work.

## 3.1. One-port model extraction methods for linear synthesis

Wideband circuit design may fail when using models, on which the element values are estimated from low frequency measurements.
The introduction [213,214] in 1967 of automated microwave network analyzers has facilitated linear transfer measurement of devices, observed relative to one or more reference planes. The blackbox methods of section 2.2 facilitate the representation of these measurements with matrix parameters for each frequency of interest. These representation methods are eminently suited to wideband circuit design, because various circuit simulators can handle matrix parameters in tabular format as easily as they handle equivalent circuit models.
This approach, although effective for computer assisted circuit analysis, is inconvenient for circuit synthesis[1]. The complexity of synthesis forces the use of models that are *as simple as possible*. It requires models with a minimum number of parameters, yet still adequate over the full frequency band of interest. This is crucial, since wideband synthesis methods rely in the main on manual interpretation of device parameters.
This work has resulted in robust algorithms for extraction of device models from measured data, suitable for (linear) synthesis. The modeling algorithms are based on the extraction of rational functions (poles and zeros) and have been proven useful in avoiding superfluous elements[2] in device models. These rational functions provide polynomial coefficients or poles and zeros that are directly related to the element values of an equivalent circuit model.
This section discusses the methods of extraction in detail.

The discussion that will follow on device modeling and parameter extraction is based on profound experience with practical measurements. This requires more than a single measurement instrument, and therefore we realized in several years a design environment for measurement, data-acquisition, analysis and synthesis. The major part of the SABEL-CAE[3] system has been described in many internal reports, and a discussion of all its aspects is beyond the scope of this text. A short overview of its application has been described in [101,109] and further in section 1.4.2.

### *3.1.1. Elementary extraction methods of analytical transfer functions*

The most elementary extraction is the determination of poles and zeros or of polynomial coefficients from transfer functions in tabular form. Let **H** and **ω** be two column vectors, representing the (measured) complex function values and their associated angular frequencies. Curve fitting with an appropriated analytical function will provide usable parameters for modeling purposes. In this section, we focus on (one of) the following target functions:

$$H_1(j\omega) = H_1(s) = \qquad a_0 + a_1 \cdot s + a_2 \cdot s^2 + ..... + a_n \cdot s^n$$

[1] The purpose of analysis is to find the properties of an extant circuit. Circuit simulations as well as measurements are adequate methods. The purpose of synthesis is to find a circuit that meets a set of pre-defined conditions. This is the reverse problem.

[2] It is not uncommon to add series inductors to all output terminals of a device model, to represent bond wires. We observed that most of these additions are superfluous in applications below 1 GHz.

[3] SABEL-CAE: Synthesis and Analysis of Broadband ELectronics, using Computer Assisted Engineering.

$$H_2(j\omega) = H_2(s) = G_\infty \cdot \frac{a_0 + a_1 \cdot s + a_2 \cdot s^2 + \ldots\ldots + a_{m-1} \cdot s^{m-1} + s^m}{b_0 + b_1 \cdot s + b_2 \cdot s^2 + \ldots\ldots + b_{n-1} \cdot s^{n-1} + s^n}$$

$$H_3(j\omega) = H_3(s) = G_0 \cdot \frac{(1-s/z_1)\cdot(1-s/z_2)\cdot(1-s/z_3)\cdot \ldots\ldots\ldots \cdot(1-s/z_m)}{(1-s/p_1)\cdot(1-s/p_2)\cdot(1-s/p_3)\cdot \ldots\ldots \cdot(1-s/p_n)}$$

$$H_4(j\omega) = H_4(s) = G_\infty \cdot \frac{a_0 + a_1 \cdot s + a_2 \cdot s^2 + \ldots\ldots + a_{m-1} \cdot s^{m-1} + s^m}{b_0 + b_1 \cdot s + b_2 \cdot s^2 + \ldots\ldots + b_{n-1} \cdot s^{n-1} + s^n} \cdot e^{-s\tau}$$

For first order estimations, a manual curve fit is adequate. It relies on the estimation of asymptotic lines of transfer functions, using the Bode plot. The corner frequency of these asymptotic lines equals the corner frequencies of a pole or a zero.

The higher the order[4] of approximation, the more the extraction relies on automated curve fitting. Some examples are:

- Automated polynomial fits (Taylor expansions) to $H_1(j\omega)$ require (non-iterative) linear extraction methods as described in appendix *C*.
- Automated rational function fits to $H_2(j\omega)$ require iterative extraction methods as described in appendix *D*. This is a new (linear) iteration method that does not require starting values. This has made the algorithm robust and simple.
- Automated pole-zero fits to $H_3(j\omega)$ are similar to rational function fits to $H_2(j\omega)$, and use an additional root finding algorithm for polynomials.
- Automated delayed pole-zero fits, to $H_4(j\omega)$, require iterative *non-linear* extraction methods. Well-known iteration algorithms, such as Levenberg-Marquardt [410,413] or Gauss-Newton [413], are applicable. The development of simpler and robust algorithms, using linear methods, is of interest for further investigation. Alternatively, a constrained rational phase fit is often applicable, as discussed in the succeeding paragraph.

Optimal curve fitting requires the minimization of some residual error term in a least squares sense. Various algorithms found in the literature minimizes some *absolute* error, such as $\varepsilon_1(j\omega) = |H(j\omega)-h(j\omega)|$ or $\varepsilon_2(j\omega) = (H(j\omega)-h(j\omega))^2$. One sometimes construct rational function approximations from a power series expansion of $h(j\omega)$. This is called Padé approximation [413]. The Remez algorithm [413] produces the best Chebyshev approximation to a given frequency response with a fixed number of filter coefficients.

We have found it more useful to minimize the *relative* error $\varepsilon(j\omega)=H(j\omega)/h(j\omega)-1$ in a least squares sense over all angular frequencies $\omega$. In this expression is $h(j\omega)$ the data table and is $H(j\omega)$ the function to be fitted. Our algorithms facilitate weighing of this relative error for enhancing curve fitting in specific frequency intervals.

The linear extraction algorithms in this section, as well as many other algorithms that will be discussed in this book, rely on methods that solve over-determined sets of linear equations. These methods use an over-determined matrix division, as described in detail in appendix *B*.

***Constrained curve fits***

[4] The approximation order is the number of roots in a polynomial fit, or the highest number of poles or zeros in a rational function fit.

Several algorithms are applicable when the magnitude as well as the phase of the transfer function is measured. The acquisition of this information is feasible with vector network analyzers, which are commercially available.
In some practical situations, however, transfer information is limited to either magnitude or phase information. This work has resulted in two additional automated extraction algorithms, as is described in appendix *E* and *F*.

- A rational magnitude fit extracts $H(j\omega)$ from $|H(j\omega)|$ in tabular format. The network is assumed to be a minimum phase network, which means that all poles and zeros have negative real part.
- A rational delay fit extracts $H(j\omega)$ as a pseudo delay transfer function. The network is assumed to be an all-pass network, which means that $|H(j\omega)|\equiv 1$

A constrained magnitude fit is required, when the transfer is measured with a spectrum analyzer using a tracking generator or white noise generator as source. Other examples are scalar network analyzer measurements.

### *3.1.2. Extraction methods for equivalent circuit elements*

Elementary transfer function curve fits generate impedance or admittance functions without regard to physical implementation. This simplifies determination of a suitable order of approximation. Pole-zero extraction methods are generally applicable to arbitrary *lumped* element models. Polynomial curve fits are of limited applicability, and are usually restricted to the extraction of dominant properties of the transfer function. Note that a *polynomial* fit of $H(j\omega)$ maps the transfer function to $\infty$ for infinite frequencies, and a fit of $1/H(j\omega)$ maps the function to zero. Polynomial curve fits are nevertheless preferred when applicable, since they are non-iterative methods.

***Polynomial fits***

When Z is a lumped impedance function, then polynomial methods are of practical applicability to the following combinations of lumped impedances:

| | |
|---|---|
| *series R and L* | $Z = R + j\omega\cdot L$ |
| *series R and C* | $j\omega\cdot Z = 1/C + j\omega\cdot R$ |
| *series R, C and L* | $j\omega\cdot Z = 1/C + j\omega\cdot R + (j\omega)^2\cdot L$ |
| *parallel R and C* | $1/Z = 1/R + j\omega\cdot C$ |
| *parallel R and L* | $j\omega/Z = 1/L + j\omega/R$ |
| *parallel R, C and L* | $j\omega/Z = 1/L + j\omega/R + (j\omega)^2\cdot C$ |

Examples are discussed in subsection 3.1.3 concerning impedance extraction of lasers and photo diodes. These examples are special situations of Taylor series. These (infinite) series are applicable when their interval of convergence spans the frequency band of interest. Unfortunately, this applies only for a limited[5] set of transfer functions.

[5] An example that illustrates when it is useless to evaluate a higher order Taylor expansion is a shunt of series impedances with R and C. The most striking aspects of overall impedance are observed near the corner

Examples of the successful use of a Taylor expansion are simple distributed models with pure delay. This is because an exp(x) function is convergent for all values x. This is demonstrated in section 3.2 in the context of transistor model extraction.
Polynomial methods are occasionally of practical applicability to functions as:

$$e^{-j\omega\tau} = 1 - j\omega\tau + 1/2\cdot(j\omega\tau)^2 - 1/6\cdot(j\omega\tau)^3 + \cdots\cdots \pm 1/n!\cdot(j\omega\tau)^n + \cdots$$
$$e^{-j\omega\tau_d}\cdot(1-j\omega\tau_0) = 1 - j\omega(\tau_0+\tau_d) + 1/2\cdot(j\omega)^2\cdot(\tau_d{}^2+2\cdot\tau_0\tau_d) + .....$$

***Rational function fits***
Pole-zero extraction methods are more generally applicable, although they require an iterative approach. A rational function fit, as described in appendix *D*, extracts the coefficients of the numerator and denominator polynomials and is relatively simple.
On the other hand, the arithmetic precision of the computer is a serious limitation in the application of the method. Using double precision (15 decimals), the ratio between the largest and smallest coefficients is limited to $10^{15}$. Adequate frequency scaling[6] will balance the polynomial coefficients to minimize this disadvantage. As a result, an extraction of rational functions with $6^{th}$-order polynomials is limited to a frequency interval not exceeding $(f_{max}/f_{min}) \approx 10^5 = \sqrt[3]{(10^{15})}$.
In exceptional situations, this interval limit is unacceptable. Alternative methods that focus directly on poles and zeros, instead of polynomial coefficients, are potentially applicable over wider frequency intervals. They are more complicated then the (linear) rational function fits and requires the use of non-linear iteration methods. Examples of these methods are Levenberg-Marquardt and Gauss-Newton, based on partial derivatives.
In summary, our linear rational extraction methods are often adequate for the extraction of models for synthesis purposes. In many applications, the non-iterative polynomial method is even adequate.

### *3.1.3. Extraction of adequate photo-diode impedance-models*

When designing lightwave receivers using feedback loops, the impedance of the photo-diode affects the loopgain transfer function. Analysis and synthesis of loop stability as well as receiver bandwidth rely on adequate models of the source impedance of this input device. This illustrates that source impedance is an important design parameter.
A first-order approximation of this source is a controlled current source, proportionally controlled by the light intensity. Its responsivity is frequency dependent. Since this responsivity does not affect the loop stability of the lightwave receiver and may by chosen to be flat over a wide frequency interval, this design parameter is of secondary importance.

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frequencies $\omega=1/RC$ of the individual shunts. Each shunt admittance equals $Y=j\omega C/(1+j\omega RC)$ and generates a Taylor expansion, similar to $x/(1+x)=x\cdot(1-x+x^2-x^3+x^4...)$. The interval of convergence begins or ends when $|x|=1$ or when $\omega<1/RC$ or $\omega>1/RC$. As a result, in this example the Taylor expansion is unable to model the most striking aspects of the transfer function and yields poor accuracy results.

6 An adequate choice of frequency $\omega_0$ balances the leading and trailing coefficients of a polynomial p(s). It equals $q_3=1$ in: $p(s) = c_0 + c_1\cdot s + c_2\cdot s^2 + c_3\cdot s^3 = c_0\cdot\{ 1 + q_1\cdot(s/\omega_0) + q_2\cdot(s/\omega_0)^2 + q_3\cdot(s/\omega_0)^3 \}$. The magnitude of one of the center coefficients will probably dominate the other coefficients.

Impedance measurements will demonstrate whether a simple impedance approximation is adequate or that higher order models are necessary. For this, it is required that the test geometry simulates the situation in which the device is connected to the circuit. For instance, a home-made PCB (printed circuit board) test-fixture shown in figure 3.1 is appropriate when the photo-diode is mounted on the edge of a PCB with microstrip layout. The photographs in figure 3.4 and 3.5 show an alternative construction in case the DUT has special mounting requirements.

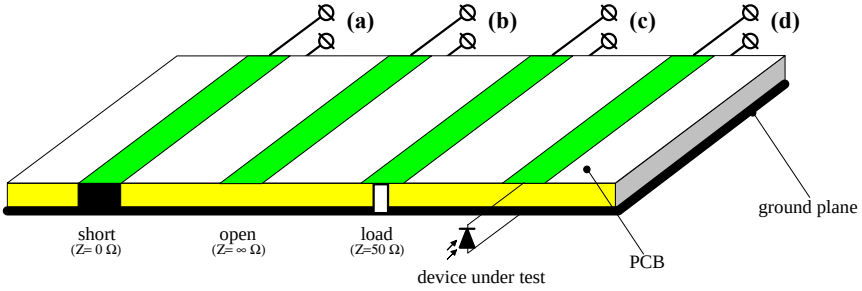


***Fig 3.1*** *Example of a test-fixture with microstrip layout to measure the impedance of photo-diodes. It is an epoxy PCB (printed circuit board) with 1.5 mm thickness, on which the device under test is mounted on the edge. Its unknown impedance is compared to three well-known impedances using a network analyzer: a Short (0 W) an Open (¥ W) and a Load (e.g. a 50 W SMD-resistor) mounted on the edge of the PCB test-fixture*

Figure 3.1 shows a simple test fixture to measure the photo-diode impedance observed relative to a reference plane that coincides with the edge of the PCB. A vector network analyzer is subsequently connected to the ports *a*, *b*, *c* and *d*, and the device impedance is extracted from all four reflection measurements and the three known impedance values. This is a standard feature on network analyzers, when calibrated with a "Short", "Open" and "Load" on port *a*, *b* and *c*.

Figure 3.2 shows the measured impedance, observed relative to the edge of the PCB test-fixture. To demonstrate the use of the impedance extraction methods in subsection 3.1.2, we applied various curve fits to this measured impedance. The following fits are shown in figure 3.2:

- A simple first order polynomial fit ($Z_1$), fitted up to 500 MHz, provides a first order approximation that is adequate up to 1 GHz.
- A second order polynomial fit ($Z_2$), fitted up to 2.2 GHz provides a model that is applicable up to 2.2 GHz.
- A third order rational function fit, fitted over the full measured frequency band provides reliable modeling up to 4 GHz.

The measured impedance illustrates a decreasing impedance with increasing frequency. This is indicative of dominant capacitive behavior.

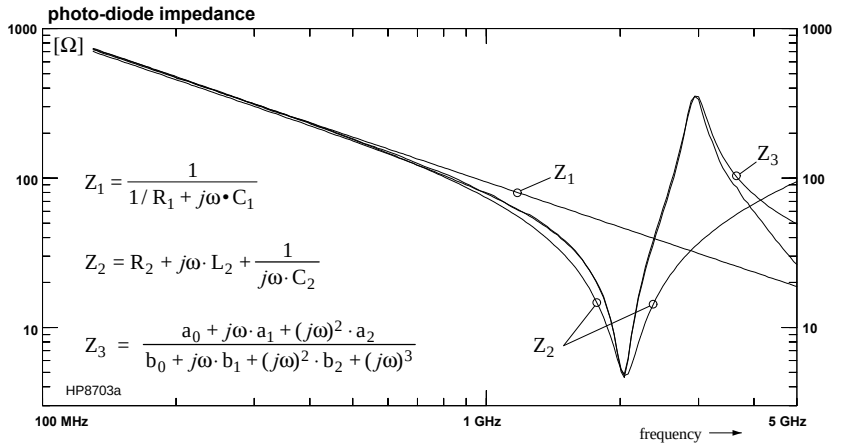


***Fig 3.2*** *Measured impedance Z of a photo-diode, observed relative to the edge of the PCB test-fixture, as is shown in figure 3.1. This function is fitted with various curves using polynomial and rational functions.*

Figure 3.3 shows some simple models of photo-diodes. The controlled current sources represent the responsivity of the photo-diode, which is frequency dependent. Nevertheless, this transfer function is commonly flat over a wide frequency band. Modeling its transfer requires additional measurements, which are not considered in this subsection.

In this example, the extracted resistance values of the shunt RC-model as well as series RC-model are not significant. This is because the influence of the (very high) shunt resistor is noticeable far below the measured frequency interval, and the influence of the (low) series resistance is negligible comparing to higher order effects. As a result, the only relevant elements in the first order models are the extracted capacitors.

On the other hand, the extracted series resistor of the series RCL model is meaningful. Variation of that value will significantly reduce the accuracy of the model.

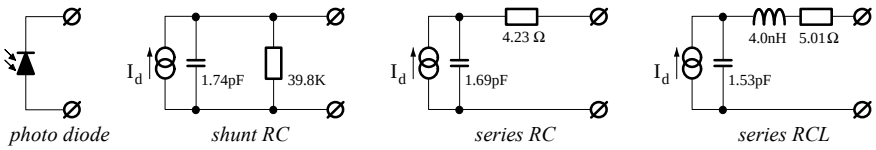


***Fig 3.16*** *Examples of simple (impedance) models of photo-diodes, extracted from the measurements in figure 3.2.*

Note that the extracted capacitor values in figure 3.3 are slightly different (10%). This demonstrates that specification of diode capacitance is model-dependent. As a result, high frequency extrapolation, based on low frequency capacitance measurements, is simply not possible. Most (higher order) curve fitting is not associated with a specific circuit topology. It illustrates rather that rational function fits serve as an intermediate step between measured data and an extracted circuit model. This approach facilitates an assessment of the value of higher order approximations, while ignoring the circuit topology required. Modeling of marginal (higher order) side effects is avoided by using

rational function fitting. As a result, our rational function approach yields the simplest equivalent circuit model, that is adequate for circuit analysis and synthesis, within the frequency band of interest.

### *3.1.4. Conclusions*

This study resulted in iteration techniques for fitting rational functions with measured data in tabular form. The algorithms are linear and require no starting values. These properties have made the algorithm robust and simple.

One-port extraction methods have been developed, for extracting device models from measured data. The methods rely on polynomial fits or on rational function fits to provide poles and zeros or polynomial coefficients. These coefficients are directly related to the element values of an equivalent circuit model.

The advantage of our extraction approach is that it tackles the complex modeling in isolation from the associated circuit topology. It facilitates an easy assessment as to the need for higher order models, limiting the extraction to the simplest model within the frequency band of interest. This advantage is crucial when extracting models for synthesis purposes.

We have demonstrated the validity of our method by extracting lumped element models of the output impedance of photo diodes. To measure this impedance, observed relative to well-defined reference planes, simple test-fixtures were developed for simulating the situation in which these devices under test are connected to circuits.

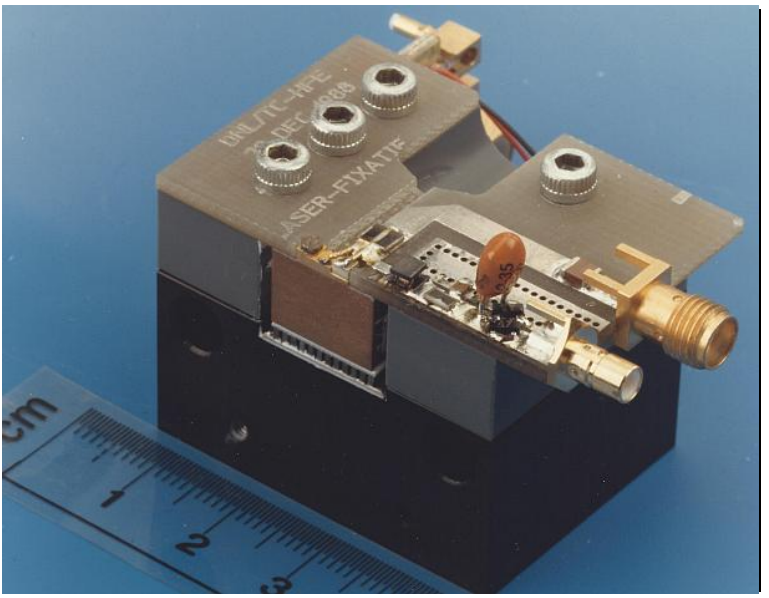


***Fig 3.4*** *Laser chip mounted in a module. Measurement of the chip impedance requires the positioning of a reference plane at the chip location.*

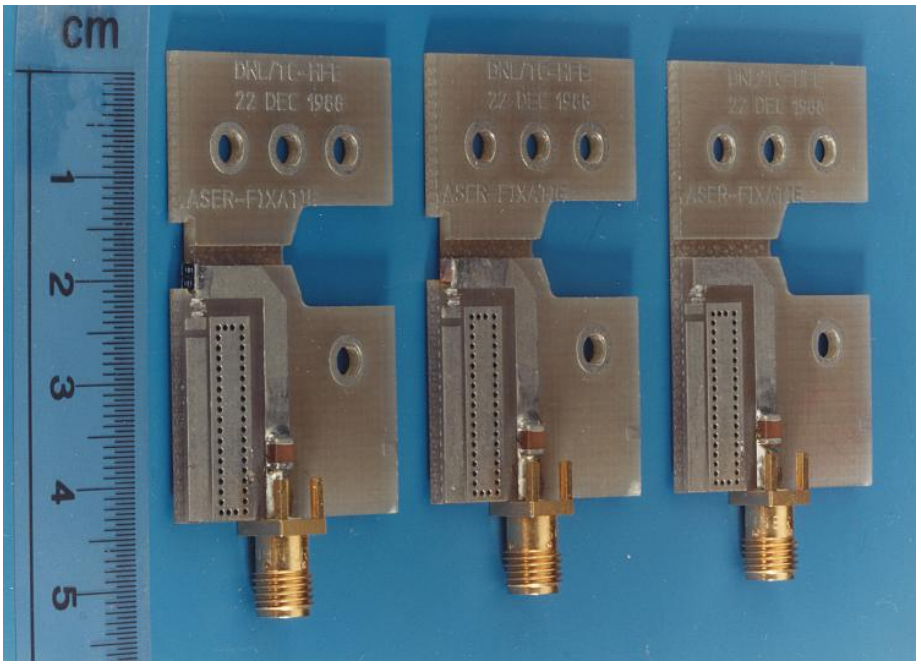


***Fig 3.5*** *Calibration setup for the laser module of figure 3.4. Three duplicate PCB's, on which the laser chip is replaced by an Open, a Short and a Load respectively, to position the reference plane at the chip location.*

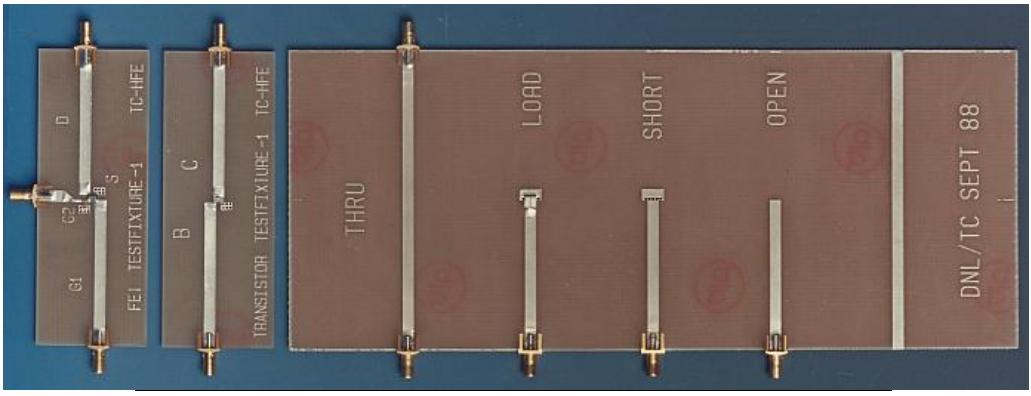


***Fig 3.6*** *Calibration setup for two-port transfer measurements on transistors. The (SMD) transistor is mounted in the center of the fixture. The symmetry of the setup facilitates the positioning of reference planes in the center of the fixture using a Load, a Short and an Open*

## 3.2. Two-port extraction methods for transistor models

Two-port extraction methods are significantly more complicated than one-port extraction methods. Moreover, the use of adequate *methods* as well as adequate *models* is far more critical. When the method fails, a solution will never be found. When the model fails, the solution is inadequate. Both possibilities will be discussed.

*A commonly used extraction method.* There are various methods to extract equivalent circuits. For instance, the commercially available software package Touchstone© [124] uses a four-dimensional iterative curve fit to fit (optimize) all relevant circuit elements of the model simultaneously with all four s-parameters of the two-port.
This brute-force method is applicable to arbitrary circuit topologies and therefore indispensable when improving sophisticated circuit models. On the other hand, the computational effort associated with the approach is very high, and the iteration may suffer from convergence problems when poor starting values are supplied.
The optimizer of Touchstone© [124] uses s-parameters as an optimization target. Usually, the relation between these parameters and the equivalent circuit elements is complex. As a result, the use of s-parameters as an optimization target can conceal the real cause when an iteration fails due to an improperly chosen circuit topology.
Wideband circuit synthesis requires equivalent models that are as simple as possible in order to be tractable for the synthesis. The use of iterative brute force methods is unnecessarily complicated when evaluating synthesis models.
This section 3.2 proposes novel extraction methods for transistor synthesis models, that are significantly simpler and require no starting values.

*A commonly used transistor model.* Adequate small-signal models of the active devices are vital for designing wideband feedback amplifiers. The well-known hybrid-Π model [304,406] is commonly considered to be particularly suitable for describing the small-signal behavior of BJT's (bipolar junction transistors) and FET's (field effect transistors). This BJT-model is based on diffusion capacitance to model its frequency response.
When designing wideband lightwave receivers, we have observed a disagreement between transfer measurements and circuit analysis when applying BJT models based on diffusion capacitance. This disagreement holds particularly for frequencies above 10% of the transition frequency $f_T$. The same disagreement was observed when applying brute force extraction methods to this conventional BJT model on measured two-port parameters. The hybrid-Π model was observed to be adequate for FET's.
To increase the predictive performance of transistor models, a considerable effort has been devoted to developing accurate and complex device models with many parameters [302,303,305]. Moreover, each minor parasitic effect, such as bond wire inductance or stray capacitance in the package, has often been taken into account in these models. This approach, while effective for analysis, is unsuitable for the purposes of synthesis.
Synthesis requires models that are made as simple as possible, without unacceptable loss in predictive performance. Models based on diffusion-capacitance are commonly used for this purpose [406], however, they become inadequate for frequencies in excess of 10% of $f_T$. This section discusses in an improved synthesis model for BJT's, and a well-known adequate synthesis model for FET's.

### *3.2.1. Virtual circuit parameters as device representation method*

Our wideband transistor models[7] rely on full two-port measurements to validate the models for the frequency interval of interest. This requires a reliable measurement method as well as an adequate way to represent the measured results. We will discuss them both.

***Measurement method***

Reliable measurements on transistors require the test geometry to simulate the situation in which the device will be connected to circuits. When using automated network analyzers, this situation is easily simulated. For instance, a home-made PCB test fixture shown in figure 3.7 is appropriate for the required two-port measurements when the transistor is mounted on the surface of the PCB. A photograph of this setup is shown in figure 3.6.

The calibration of the network analyzer requires an "Open", "Short" and "Load", similar to the construction of figure 3.1. They have been realized by halving a duplicate test-fixture, and mounting the reference impedances on the edge of the PCB, to position the reference plane in the center of the transistor fixture. A calibrating "Thru" has been realized using another duplicate fixture, with a through-connection in the center.

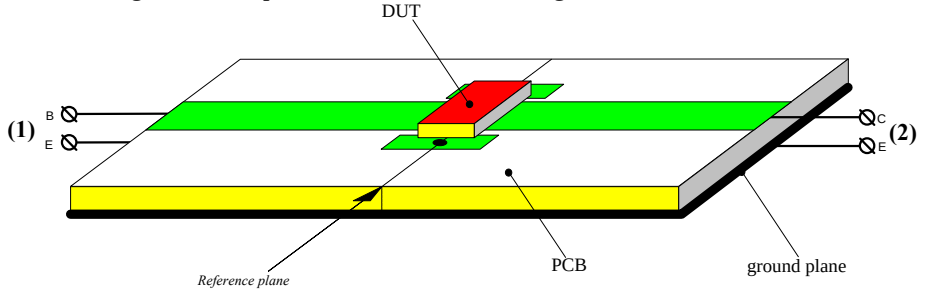


***Fig 3.16*** *Example of a test-fixture with microstrip layout to measure the two-port parameters of transistors. It is an epoxy PCB (printed circuit board) with 1.5 mm thickness, on which the DUT (device under test) is mounted on the surface of the PCB. Via holes connect the emitter contact with the ground-plane on the bottom side.*

***BJT example***

Commercially available network analyzers determine two-port parameters in s-parameter format. We prefer virtual circuit parameters as a representation method (see section 2.3.2) to simplify interpretation and model extraction. The virtual circuit parameters are converted from s-parameters, using y-parameters as an intermediate step. Figure 3.8 shows[8] measured[9] virtual BJT-parameters [$\alpha_b$, $z_e$, $z_{ce}$, $z_{cb}$] of a bipolar junction transistor. The magnitude of the current gain $\alpha_e$ in figure 3.8a illustrates that the transition frequency $f_T$ is approximately 3.5 GHz. This is estimated from the frequency where the current gain parameter $\alpha_e$ has been reduced to $|\alpha_e|=1$. See section 2.3.2 for the definition of the virtual circuit parameter $\alpha_e$.

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[7] All our transistor modelling effort was restricted to (linear) small signal models

[8] The measured curves are overlayed with curves predicted by a BJT-model, as discussed in subsection 3.2.2.

[9] In fact, the *s-parameters* of the BJT are measured, and the virtual BJT parameters are extracted from them.

Figure 3.8b shows the phase of $\alpha_b$ and $\alpha_e$ converted from measured s-parameter data. These plots illustrates that our BJT-model provides an excellent fit with the measured phase over the full frequency band. The associated phase-delay and group-delay[10] (not shown in this plot) are almost frequency independent.
Figure 3.8c and 3.8d show the three impedance values of the virtual BJT-parameters. These curves provide an excellent fit for $z_e$ and $z_{cb}$ and a fair fit for $z_{ce}$. This demonstrates the validity of our BJT model.

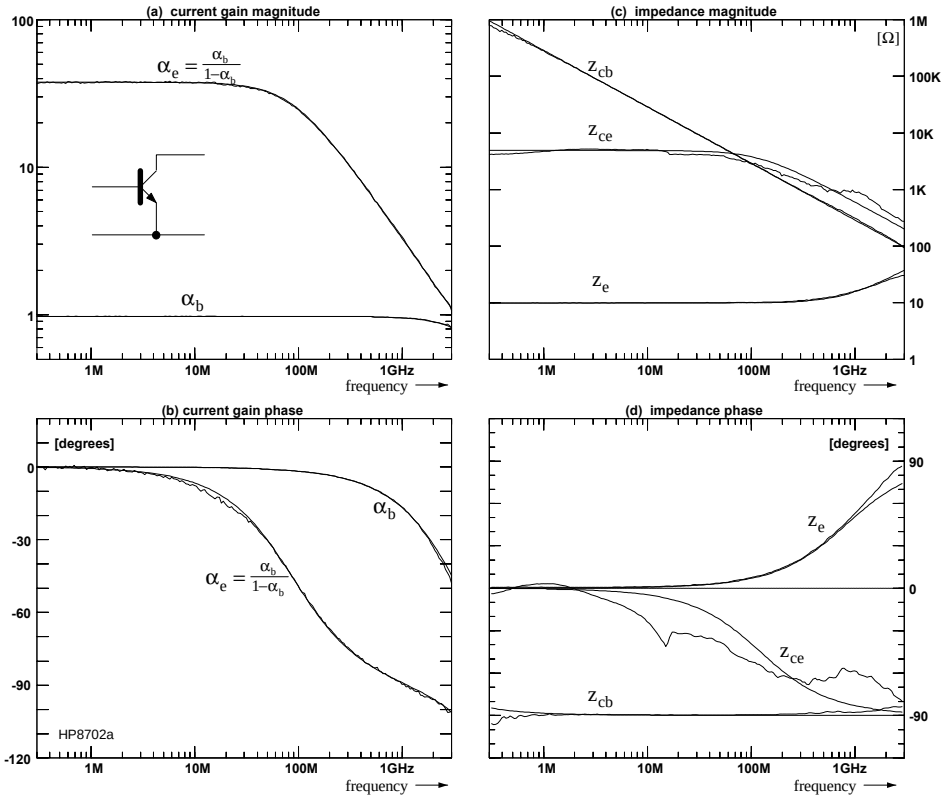



***Fig 3.16*** *Virtual circuit-parameter plots to represent the measured two-port parameters of a bipolar junction transistor. These parameters are defined in section 2.3.2. The dotted lines are converted from measured s-parameter data (201 frequency points), and the solid lines are predicted by the BJT model proposed in figure 3.10. That model is more adequate than the well-known hybrid* Π *-model, as discussed in section 3.3.2.*

### *FET example*

Figure 3.9 shows measured virtual FET-parameters [$g_m$, $z_{gs}$, $z_{ds}$, $z_{dg}$] of a field effect transistor (CF910: dual-gate GaAs-MesFET), superimposed on predicted virtual parameters using a hybrid-Π model. These parameters are slightly different from virtual BJT parameters, however, a similar approach applies.

[10] The phase delay of phase $\varphi(\omega)$ is defined as: $\tau_{dp} = -\frac{\varphi}{\omega}$, and the group delay is defined as $\tau_{dg} = -\frac{d\varphi}{d\omega}$

The curves in figure 3.9a and 3.9b demonstrate an excellent fit for the transconductance $g_m$over the full frequency band. The associated phase-delay and group delay (not shown in this plot) are almost frequency independent.
A similar resemblance applies for the reconstructed impedances $z_{dg}$ and $z_{gs}$ in figure 3.9c and 3.9d, although the poor resemblance of their phase suggests the contrary. This is a seeming contradiction since $z_{gs}$ and $z_{dg}$ represent very weak effects, especially at low frequencies, because their shunt impedance is very high. Measurement of these weak effects is beyond the accuracy limits of the used measurement setup.

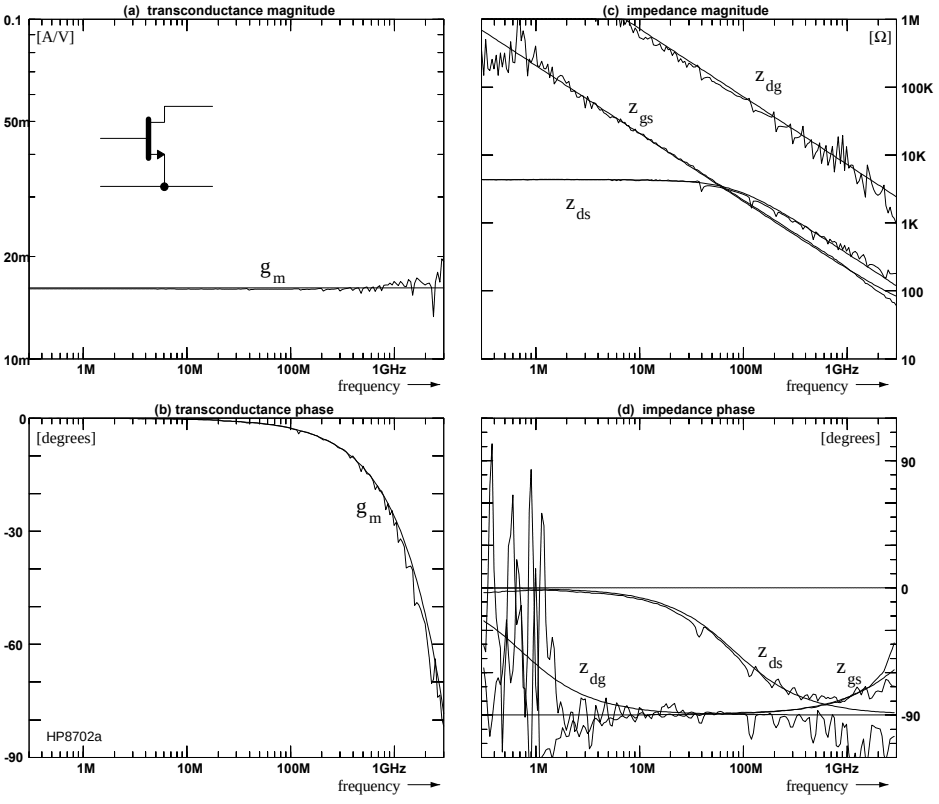



***Fig 3.16*** *Virtual circuit-parameter plots to represent the measured two-port parameters of a field effect transistor. These parameters are defined in section 2.3.2. The dotted lines are converted from measured s-parameter data (201 frequency points), and the solid lines are predicted by the FET model shown in figure 3.11.*

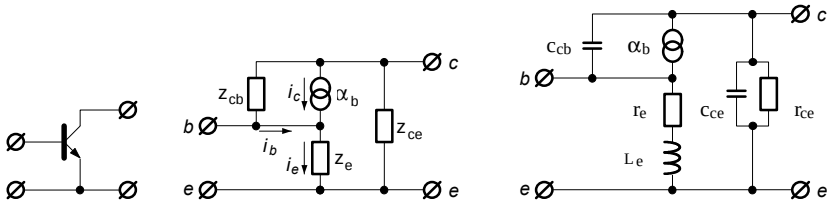
### *3.2.2. Extraction of transistor parameters using Taylor series expansion*

Brute force methods use a four-dimensional iteration for fitting all two-port parameters simultaneously with the model. We developed an alternative method that use four *individual* one-dimensional fits. It is applicable to transistors when using adequate virtual circuit parameters as two-port representation.

Our approach is significantly simpler and normally requires no iteration at all. It consists of the following steps:

- First, transform the measured two-port parameters to a virtual circuit-parameter format that is closely related to the circuit topology of interest. For transistors, these parameters are defined in section 2.3.2 and examples are shown in figure 3.8 and 3.9.
- Fit each virtual circuit parameter individually with a simple rational or polynomial function. This approach provides (polynomial) coefficients that are closely related to the circuit elements of an intrinsic circuit model.
- If this intrinsic circuit model is inadequate for the frequency interval of interest, extend the model with additional elements. Use the element values of the intrinsic model as starting values in a four-dimensional iteration.

In our experience, the first two steps are often adequate for transistor model extraction. Furthermore, it is observed that simple polynomials (Taylor series, expanded to one or two power terms) are often adequate for fitting measured virtual circuit parameters. This provides the means to define the most significant transistor parameters in an unambiguous way. Extraction of these parameters is performed in a similar way.

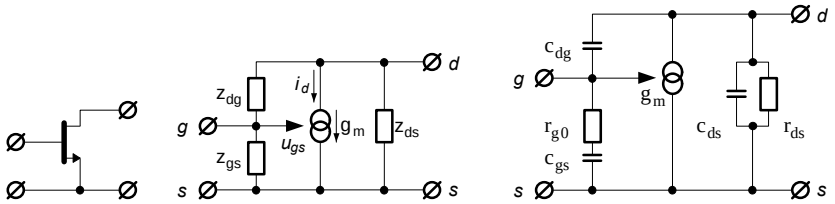



| | | |
|---|---|---|
| $1/\alpha_b$ | $= (y_{11}+y_{21})/(y_{21}-y_{12})$ | $= 1/\alpha_{b0} + j\omega/\omega_{T1} + (j\omega/\omega_{T2})^2 + \ldots$ |
| $1/\alpha_e$ | $= (y_{11}+y_{12})/(y_{21}-y_{12})$ | $= 1/\alpha_{e0} + j\omega/\omega_{T1} + (j\omega/\omega_{T2})^2 + \ldots$ |
| $z_e$ | $= 1/(y_{11}+y_{21})$ | $= r_e + j\omega \cdot L_e + \ldots$ |
| $1/z_{ce}$ | $= y_{22}+y_{12}$ | $= 1/r_{ce} + j\omega \cdot c_{ce} + \ldots$ |
| $1/z_{cb}$ | $= -y_{12}$ | $= 1/r_{cb} + j\omega \cdot c_{cb} + \ldots$ |

***Fig 3.16*** *Simple BJT transistor model of which the parameters can easily be extracted from Taylor expansions of measured two-port parameters transformed to virtual BJT parameters. We define:* $\omega_T = \omega_{T1}/\alpha_{b0} = 2\pi \cdot f_T$, $\omega_e = r_e/L_e$ *and* $c_e = 1/(r_e \cdot \omega_T)$. *Note that* $1/\alpha_b = 1/\alpha_e + 1$.

The equations in figure 3.10 define the most significant parameters of bipolar junction transistors as the coefficients of a Taylor expansion of the associated virtual circuit parameters. They are directly applicable in equivalent circuit models. Furthermore, they illustrate the advantages of using virtual circuit-parameter plots as a device representation method. The most significant transistor parameters are directly obtainable from graphical interpretation of the logarithmic plots using their asymptotic slopes.

Figure 3.11 provides similar definitions for field effect transistors. Note that the expansion for $z_{gs}$ is, strictly speaking, a MacLaurin expansion.




$$g_m = y_{21} - y_{12} = g_{m0} + j\omega \cdot c_m + \ldots$$
$$j\omega \cdot z_{gs} = j\omega/(y_{11}+y_{12}) = 1/c_{gs} + j\omega \cdot r_{g0} + \ldots$$
$$1/z_{ds} = y_{22}+y_{12} = 1/r_{ds} + j\omega \cdot c_{ds} + \ldots$$
$$1/z_{dg} = -y_{12} = 1/r_{dg} + j\omega \cdot c_{dg} + \ldots$$

***Fig 3.16*** *Simple FET transistor model of which the parameters can easily be extracted from Taylor expansions of measured two-port parameters transformed to virtual FET parameters.*
*We define:* $\omega_T = g_m/(c_{gs}+c_{dg})$

In figure 3.8 and 3.9 we demonstrated that simple Taylor series expansion of transistor parameters are applicable over a very wide frequency band. Furthermore, we have observed this for a variety of wide band transistors. An example is shown in figure 3.12, under varying the bias conditions.

***BFR92A*** *NPN bipolar transistor*

| $I_c$ | 2 | 5 | 10 | 20 | 2 | 5 | 10 | 20 | mA | |
|---|---|---|---|---|---|---|---|---|---|---|
| $U_{ce}$ | 5 | 5 | 5 | 5 | 10 | 10 | 10 | 10 | V | |
| $\alpha_{e0}$ | 68.949 | 73.153 | 78.993 | 83.133 | 75.435 | 81.664 | 90.139 | 103.066 | --- | |
| $f_T$ | 2.972 | 4.895 | 6.245 | 6.865 | 2.937 | 4.874 | 6.265 | 6.910 | GHz | |
| $\tau_{\alpha 0}$ | 16.085 | 42.075 | 65.907 | 100.000 | 18.477 | 37.722 | 100.000 | 100.000 | % | see |
| $\tau_{\alpha 1}$ | 83.915 | 57.925 | 34.093 | 0.000 | 81.523 | 62.278 | 0.000 | 0.000 | % | section |
| $r_e$ | 12.364 | 5.883 | 3.464 | 2.220 | 12.884 | 6.198 | 3.766 | 2.529 | Ω | 3.2.3 |
| $L_e$ | 1.426 | 1.531 | 1.526 | 1.530 | 1.434 | 1.549 | 1.552 | 1.563 | nH | |
| $r_{ce}$ | 34.655 | 20.322 | 9.877 | 7.246 | 64.433 | 64.027 | 10.727 | 8.373 | kΩ | |
| $c_{ce}$ | 0.230 | 0.240 | 0.243 | 0.243 | 0.232 | 0.234 | 0.218 | 0.228 | pF | |
| $c_{cb}$ | 0.424 | 0.421 | 0.418 | 0.424 | 0.392 | 0.394 | 0.397 | 0.400 | pF | |
| $f_T/\alpha_{e0}$ | 43.100 | 66.918 | 79.057 | 82.576 | 38.930 | 59.685 | 69.501 | 67.041 | MHz | |
| $f_{T1}$ | 2.929 | 4.829 | 6.167 | 6.783 | 2.898 | 4.815 | 6.196 | 6.843 | GHz | $= \omega_{T1}/2\pi$ |
| $f_{T2}$ | 7.671 | 8.435 | 9.336 | 9.334 | 7.124 | 8.757 | 8.800 | 9.159 | GHz | $= \omega_{T2}/2\pi$ |
| $f_e$ | 1.380 | 0.612 | 0.361 | 0.231 | 1.430 | 0.637 | 0.386 | 0.257 | GHz | |
| $c_e$ | 4.332 | 5.527 | 7.357 | 10.444 | 4.206 | 5.268 | 6.747 | 9.108 | pF | |

***Fig 3.12*** *Example of extracted transistor parameters, using the s-parameters as specified by the manufacturer (Philips). Note that all values* $r_e$ *are approximately 1.3*Ω *higher then is expected from the bias current* $I_c$*. This is due to emitter series resistance, which is roughly independent of the bias current.*

### *3.2.3. Extraction of parameters with delay using Taylor series expansion*

The validity of the transistor models in figure 3.10 and 3.11 can be improved when modeling the gain transfer functions as the cascade of a low-pass transfer function and a delay function. The modified transfer functions becomes:

*BJT*: $$\alpha_b = \frac{\alpha_{b0}}{(1+j\omega\cdot\tau_{\alpha1} + \ldots)} \cdot e^{-j\omega\cdot\tau_{\alpha0}}$$

*FET*: $$g_m = \frac{g_{m0}}{(1+j\omega\cdot\tau_{g1} + \ldots)} \cdot e^{-j\omega\cdot\tau_{g0}}$$

One way to extract these modified gain transfer functions is by using an iterative curve fit to the proposed function. A simpler (non-iterative) way is evaluating a Taylor expansion and using the extracted coefficients for calculating the modified delay coefficients. Delay is represented by infinite Taylor series, however, it can be reconstructed when the first terms of the expansion are known. For instance, when the expansion of $\alpha_b$ is restricted to the first three terms, it provides the coefficients ($\alpha_{b0}$, $\omega_{T1}$, $\omega_{T2}$) as defined in subsection 3.2.2. These parameters are related as follows to the modified delay coefficients ($\tau_{\alpha0}$, $\tau_{\alpha1}$):

*BJT*: $$\frac{\alpha_{b0}}{\omega_{T1}} = \tau_{\alpha0}+\tau_{\alpha1} \qquad \frac{\alpha_{b0}}{(\omega_{T2})^2} = \tau_{\alpha0}\cdot\tau_{\alpha1} + \tfrac{1}{2}\cdot(\tau_{\alpha0})^2$$

Modeling with additional delay may improve the gain transfer function for frequencies near the transition frequency $\omega_T$. This is illustrated in figure 3.13 for the current transport factor $\alpha_b$ of a 1 GHz transistor. In these plots, the delay ($\tau_{\alpha0}$) is varied while the (reciprocal) transition frequency $1/\omega_T = \alpha_{b0}/\omega_{T1} = (\tau_{\alpha0}+\tau_{\alpha1})$ is kept constant. Three distinct curves are plotted in figure 3.13:

| | | | |
|---|---|---|---|
| A: | for $\tau_{\alpha0}=0$ | and $\tau_{\alpha1}=1/\omega_T$ | (low pass transfer) |
| B: | for $\tau_{\alpha0}=0.5/\omega_T$ | and $\tau_{\alpha1}=0.5/\omega_T$ | (mixed delay and low-pass) |
| C: | for $\tau_{\alpha0}=1/\omega_T$ | and $\tau_{\alpha1}=0$ | (delayed transfer) |

All curves A, B and C have equal magnitude response and equal phase delay for frequencies below 10% of the transition frequency. The more phase delay is originating from pure delay, the less frequency dependency is observed in magnitude response and in phase delay.

The current gain plots in figure 3.8a and 3.8b show that the current transport factor $\alpha_b$ of a BJT differs from a simple first order low-pass response. A second order Taylor expansion provides accurate modeling results ($f_{T1}$=3.26 GHz, $f_{T2}$=6.86 GHz) within the measured frequency interval. The same applies for a first order Taylor expansion with additional delay. In this example the highest measurement frequency is too low to assess whether models with delayed gain are more appropriate or not.
When converting the second order Taylor expansion to a first order variant we observed that 27% of the total phase delay in $\alpha_b$ originated from pure delay while the remaining 73% originated from the phase shift in the low-pass transfer function. These ratios are bias and device dependent, as is shown in figure 3.12. Investigation of this ratio for various transistors, has shown that delay aspects dominate for high bias currents.

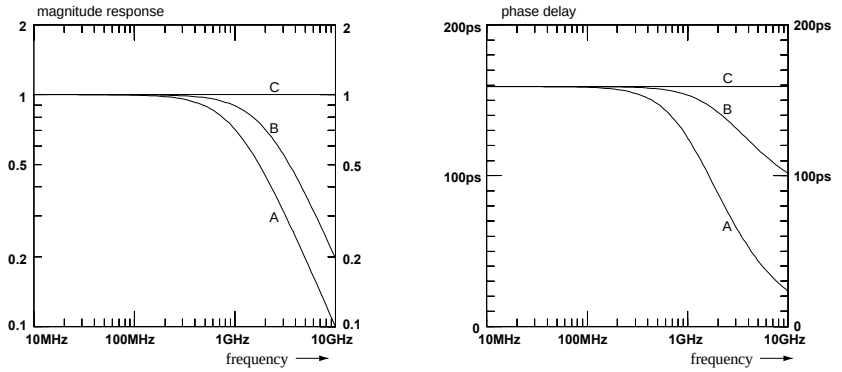



***Fig 3.16*** *Simulated current transport factor $\alpha_b$ of different bipolar junction transistors with equal transition frequency (1 GHz). Curve A illustrates when $\alpha_b$ is modeled by a first order low-pass transfer. Curve C result from a model with pure delay, while curve B is a mix from low-pass transfer and delay.*

### *3.2.4. Conclusions*

An attractive graphic method has been discussed for representing measured two-port parameters of transistors. We illustrated the advantages of using these virtual circuit-parameter plots as a device representation method. Most significant transistor parameters are directly obtainable from graphic interpretation of these logarithmic plots using their asymptotic slopes.

Transistor models for (linear) synthesis must be as simple as possible. Over-simplified as well as unnecessary complicated models are inadequate to the job and therefore they must be based on two-port measurements within the frequency band of interest.

A new extraction method has been developed and demonstrated for modeling transistors (BJT's and FET's). Our approach, using virtual circuit parameters as linear two-port description, significantly simplifies two-port modeling. It transforms an all-in-one four-dimensional curve fitting into four simple one-dimensional curve fitting procedures.

In many situations, we have observed that our approach requires no iterations at all, since polynomial fits (Taylor series) are adequate. This observation provides the means for defining the most significant transistor parameters in an unambiguous way.

On occasion, our one-dimensional approach is unable to extract adequate transistor models. In these situations, our approach is a suitable intermediate step for providing excellent starting values to brute-force four-dimensional curve fits.

## 3.3. Discussion on commonly used transistor models

The two-port extraction methods of section 3.2.2 and 3.2.3 resulted in a non-conventional model for bipolar junction transistors. Commonly used BJT models are extended with base resistance and rely on diffusion capacitance in stead of delay. This section discusses these differences.

### *3.3.1. Discussion on base resistance versus emitter inductance*

The virtual circuit parameter $z_e$ for bipolar junction transistors, as defined in section 2.3.2, is often inductive in nature. One way to model this effect is a series emitter inductor (bonding wires), as illustrated in figure 3.14a. Another way is modeling an inductive $z_e$ parameter with a series base resistor, as illustrated in figure 3.14b.
Both models are associated with equal $\alpha_e$, $z_{ce}$ and $z_{cb}$ parameter values, and similar values for the $z_e$ parameter: A first order Taylor approximation for $z_e$ yields:

*model in figure 3.14a:* $z_e \approx r_e + j\omega \cdot L_e$

*model in figure 3.14b:* $z_e \approx (r_{e0} + r_{b0}/\alpha_{e0}) + j\omega \cdot (r_{b0}/\omega_T)$

In practical situations, for instance the transistor example in figure 3.8, the differences are small. Linear two-port transfer measurements alone are usually inadequate to distinct whether inductive $z_e$ effects are to be assigned to emitter inductance, to base resistance or to a mix of both. We prefer modeling with emitter inductance to simplify the overall circuit analysis.

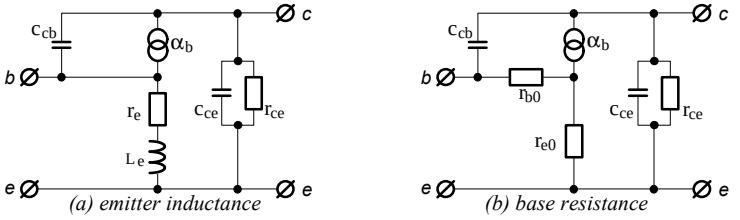



***Fig 3.16*** *Example of two different equivalent T-models for bipolar junction transistors. Emitter inductance (a) as well as base resistance (b) is capable of modeling inductive effects in the virtual circuit parameter $z_e$ (defined in section 2.3.2) of bipolar junction transistors. Both T-models have equal values for the parameter $\alpha_e$ $z_{ce}$ and $z_{cb}$, and comparative values for $z_e$.*

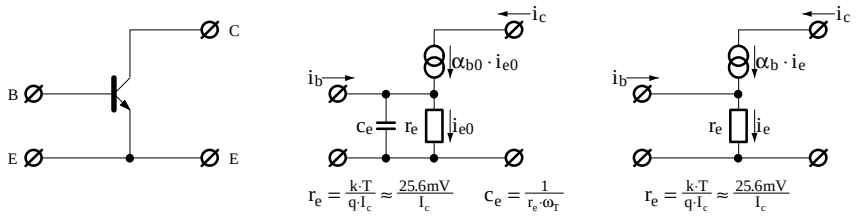
When BJT- models with base resistance are preferred, the model in figure 3.10 is to be considered as an intermediate step. This is because its parameter values $r_e$ and $L_e$ are extracted in a structured and unambiguous way. The emitter inductance variant is subsequently transformed into a base resistance variant using the transformation:

$$r_{b0} = L_e \cdot \omega_T$$
$$r_{e0} = r_e - L_e \cdot \omega_T / \alpha_{e0}$$

### *3.3.2. Discussion on current transport function vs. diffusion capacitance*

The *overall* current gain of a bipolar junction transistor is low-pass in nature (injected in the input using a current source and sensed at the output when shorted). Our transistor model of figure 3.10 uses a controlled current source $\alpha_b$ to model this effect with frequency dependent current transport factor. This is stressed in figure 3.15c. Diffusion capacitance, as shown in figure 3.15b, is another way to model a low-pass overall current gain. Nevertheless, the overall input impedance of both models are different,

which means that at least one of these models is inadequate. This subsection discusses both concepts.




*(a) bipolar junction transistor (b) diffusion capacitance concept (c) current transport concept*

| | ***diffusion capacitance concept*** $\omega_T,\ r_e,\ \alpha_{b0}$ | | ***current transport concept*** $\omega_T,\ r_e,\ \alpha_{b0}$ | | |
|---|---|---|---|---|---|
| *definition* | *relation* | *transfer* | *relation* | *pure low-pass* | *pure delay* |
| $\alpha_b = \frac{i_c}{i_e}$ | $\alpha_b = \frac{\alpha_e}{1+\alpha_e}$ | $= \frac{\alpha_{b0}}{1 + j\omega/\omega_T}$ | $\alpha_b = \frac{\alpha_e}{1+\alpha_e}$ | $= \frac{\alpha_{b0}}{1 + j\omega/\omega_T}$ | $= \alpha_{b0} \cdot e^{-j\omega/\omega_T}$ |
| $\alpha_e = \frac{i_c}{i_b}$ | $\alpha_e = \frac{\alpha_b}{1-\alpha_b}$ | $\frac{\alpha_{b0}}{1 - \alpha_{b0} + j\omega/\omega_T}$ | $\alpha_e = \frac{\alpha_b}{1-\alpha_b}$ | $\frac{\alpha_{b0}}{1 - \alpha_{b0} + j\omega/\omega_T}$ | $\frac{\alpha_{b0}}{e^{+j\omega/\omega_T} - \alpha_{b0}}$ |
| $Z_i = \frac{u_{be}}{i_b}$ | $Z_i = r_e \cdot \alpha_e / \alpha_{b0}$ | $\frac{r_e}{1 - \alpha_{b0} + j\omega/\omega_T}$ | $Z_i = r_e \cdot (\alpha_e + 1)$ | $\frac{r_e \cdot (1 + j\omega/\omega_T)}{1 - \alpha_{b0} + j\omega/\omega_T}$ | $\frac{r_e}{1 - \alpha_{b0} \cdot e^{-j\omega/\omega_T}}$ |

***Fig 3.16*** *Two essentially different modeling concepts for the BJT (bipolar junction transistor). Additional refinements, such as emitter inductance, base resistance and depletion layer capacitors, are omitted.*

- *The diffusion capacitance concept uses a frequency <u>in</u>dependent current source that senses the current flow through a resistor. An additional (diffusion) capacitor decreases the gain with increasing frequency.*
- *The current transport concept uses a frequency dependent controlled source that senses the current through a resistor. This transfer is usually a mix of delay and a low-pass transfer. Capacitors are not required for modeling the frequency response.*

*The current flow through* $r_e$ *is proportional to the voltage between base and emitter. Therefore, many authors prefer the well-known hybrid-*Π *variant of the T-model that relies on diffusion capacitance.*

The well-known hybrid-Π models, in which (diffusion) capacitance dominates the frequency response of bipolar transistors, are generally considered to be particularly suitable for describing theirs (linear) small-signal behavior [406]. Moreover, it can be concluded from microwave textbook discussions [301] that this assumption holds for multi-GHz frequencies. In our experience, BJT models dominantly based on (diffusion) capacitance become inadequate for the job for frequencies in excess of 10% of the transition frequency $f_T$.

When capacitive effects characterize the dominant frequency response, impedance $z_e$ in figure 3.10 must be a real impedance that becomes capacitive for frequencies approaching the transition frequency $f_T$. Figure 3.8c illustrates that the virtual circuit parameter $z_e$ is *inductive* rather then capacitive. From this we conclude that diffusion

capacitance is merely the result of first order approximations of BJT models up to $f_T/10$ then an adequate parameter for describing wideband transistor aspects.[11]

In our experience, the *current transport factor* is the most convenient parameter to model the dominant frequency response of bipolar transistors in an adequate but simple way. This is the virtual parameter of $\alpha_b$ in figure 3.10, as has been extracted from measured data in section 3.2.2 and 3.2.3. The excellent fitting in figure 3.8 of $\alpha_b$ and $\alpha_e$ demonstrates the validity of this concept up to $f_T$.
Figure 3.15 illustrates the elementary modeling concepts for BJT's. The model in figure 3.15b is based on (diffusion) capacitance $c_e$ and the model in figure 3.15b on a current transport function $\alpha_b$. Additional refinements, such as base resistance, emitter resistance[12] and depletion layer capacitors are omitted to simplify this inter-comparison.

***Diffusion capacitance concept***
When the diffusion capacitance is a dominant effect, the virtual circuit impedance $z_e$ must be shunted with a capacitor $c_e$ in order to affect the frequency response significantly. Using the well-known relations $\omega_t \approx 1/(r_e \cdot c_e)$, and $r_e=(kT/q \cdot I_c)$, diffusion capacitance of $c_e \approx 5$ pF would have been expected based on transition frequency ($f_T$=3.5 GHz) and bias current ($I_c$=3 mA).
Figure 3.8c illustrates that $z_e$ is *inductive* instead of capacitive. This 1.9 nH series inductor is probably caused by the emitter bond wire, and models a small parasitic effect. When some capacitive effect is noticed above $f_T$ then its value is significantly smaller than the presumed diffusion capacitor $c_e$. In fact, we do not observe any dominant capacitance effect at all!
We verified this observation for various BJT's, using the s-parameters specified by the manufacturer[13]. The emitter impedance $z_e$ is significantly inductive for all these devices, with an exception when the bias current $I_c$ is less then 1 mA. When using relatively small bias currents, the value of $r_e$ is relatively high. In these situations, a series inductor $L_e$ is too small to be noticed below the transition frequency, and a small shunt capacitor dominates the frequency response. As a result, $z_e$ is weakly capacitive for small bias currents due to the depletion layer capacitance.
From this observation, it is concluded that the junction capacitance between base and emitter is the most significant capacitor, which is usually very small and roughly independent of the bias current. As a result, the validity of BJT models based on diffusion capacitance concepts is restricted to frequencies below $f_T/10$.

[11] Naturally, improved fittings may result when fitting transistor models using more nodes and elements then is used in the equivalent circuit of figure 3.10. This has not been investigated because we prefer the simplest models.

[12] The actual value of $r_e$ is somewhat higher then expected from predictions on the collector bias current. We observed an additional value ($r_{e0} \approx 1.3\Omega$) for the BJT examples in figure 3.8 and 3.12. This resistance remains roughly constant when the bias current is varied, as is demonstrated in figure 3.12. We conclude that this offset value is caused by emitter series resistance.

[13] Philips: BF547, BF747, BFQ67, BFR92a, BFR93a, BFR106, BFR505, BFR520, BFR540, BFS17a, BFT25, BFT25a, BFT92, and BFT93.

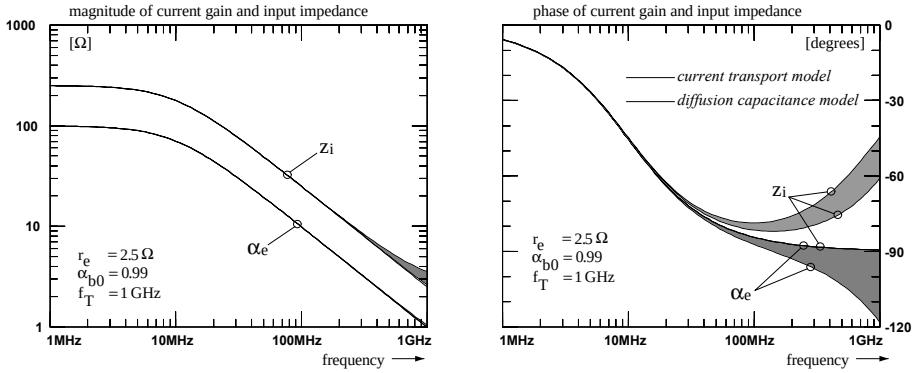



***Fig 3.16*** *Simulated differences between BJT models dominantly based on the diffusion capacitance concept and on the current transport concept, as defined in figure 3.15. Either concepts predict similar magnitude responses however the phase prediction differs significantly for frequencies above* $f_T/10$. *The shaded area's demarcate the ranges for* $\alpha_e$ *and* $z_i$ *when the current transfer in* $\alpha_b$ *varies from pure delay to first order low-pass transfer. The actual current gain is usually a mix of both transfer functions.*

***Current transport concept***

The BJT models we proposed in section 3.2.2 is fundamentally different. The basic concept, as shown in figure 3.15c, assumes all elements to be frequency independent except for the current transport factor $\alpha_b$. This concept is known from the very beginning of the transistor [205: page 190], but dropped into disuse.

For a wide range of BJT's, this concept is valid up to $f_T$. It is as simple as the commonly used diffusion capacitance concept, which is convenient for synthesis purposes.

Figure 3.16 shows simulated plots of current gain $\alpha_e$ and input impedance $z_i$. to compare either models. For frequencies up to $f_T$, the magnitude responses $|\alpha_e|$ are practically equal for both models. The same applies for $|z_i|$. Differences are mainly restricted to the phase response for frequencies above $f_T/10$.

The actual phase shift in $\alpha_e$ is higher then predicted from models based on diffusion capacitance. This difference is essential when simulating wideband feedback amplifiers since linear models based on diffusion capacitance concepts may incorrectly predict stable operation of oscillatory amplifiers.

### *3.3.3. Conclusions*

We demonstrated that the well-known hybrid-Π model, in which (diffusion) capacitance dominates the frequency response of BJT's, becomes inadequate for frequencies in excess of 10% of the transition frequency $f_T$. This is accentuated by the fact that the dominant behavior of the virtual emitter impedance $z_e$ is inductive in stead of capacitive, for various wide band transistors biased between 1 mA and 20 mA. An improved linear BJT model has been developed, applicable up to $f_T$ and suitable for synthesis. In this model, the current transport factor $\alpha_b$ dominates the frequency response. This improved model is essential when designing wideband feedback amplifiers, since it correctly predicts unstable operation of oscillatory amplifiers.